IN THE SPECIFICATION:

Please replace the text of the Background of the Invention and the text of the Detailed Description of the Preferred Embodiments. Replacement sections are attached along with marked up sections identifying the changes.

IN THE CLAIMS:

Please cancel claims 11, 12 and 18 without prejudice.

Please replace the text of claims 10, 17, 19-21 with the following text:

10. (Amended) A method for controlling a memory system which includes:

logical blocks managed by the system;

physical blocks for storing therein data corresponding to said logical blocks, said physical blocks comprising a plurality of memory cells;

redundant divisions included in corresponding ones of said physical blocks for storing therein addresses of corresponding ones of said logical blocks; and

physical block areas formed by at least two of said physical blocks,

the method including preparing a logical address/physical address translation table for managing corresponding relationships between said logical blocks and said physical block areas.

17. (Amended) A method for controlling a non-volatile semiconductor memory system, which comprises the steps of:

dividing a cell array into a plurality of physical blocks;

storing information corresponding to each relationship between said physical block and corresponding one of logical blocks which are managed by said system, in each said physical block; and

forming a table for managing corresponding relationships between said logical blocks and said physical blocks in a random access memory in said system by

sequentially preparing required corresponding relationships between said logical blocks and a plurality of physical block areas each including one or more of said physical blocks, in said random access memory in said system in accordance with accesses from a host.

19. A method for controlling a non-volatile semiconductor memory system which comprises the steps of:

dividing a cell array of non-volatile semiconductor memory cells into a plurality of physical blocks,

storing address mapping information between said physical block and a corresponding logical block in each of said physical blocks, which logical blocks are managed by said system,

forming a plurality of areas, each area being formed by an aggregate of at least one of said plurality of physical blocks,

controlling said system so that data in a logical block are stored in physical blocks defined by one of said areas, and

forming an address translation table corresponding to said area in which data in said logical block are stored when said non-volatile semiconductor memory is accessed.

20. A method for controlling a non-volatile semiconductor memory system which comprises the steps of:

dividing a cell array of non-volatile memory cells into a plurality of physical blocks;

storing address mapping information between said physical block and a corresponding logical block in a storage region of each of said physical blocks, which logical blocks are managed by said system; and

forming a table for managing a corresponding relationship between said logical blocks and said physical blocks of a flash memory, in a random access

memory of said memory system,

said method further comprising the steps of:

defining an area formed by one or more of said physical blocks,

searching said storage regions of physical blocks associated with said area,

forming said table for managing said address mapping information between said logical blocks and said physical blocks, on said random access memory of said system, and

allowing to select physical blocks corresponding to said logical blocks by using said table.

21. A method for controlling a non-volatile semiconductor memory system, as set forth in claim 20, which further comprises the steps of:

providing a function of selectively replacing a defective physical blocks including defective cells with redundant physical blocks; and

managing said function, for said each area, so that the number of defective physical blocks is less than or equal to a predetermined number.

REMARKS:

This is in response to the Office Action dated September 19, 2000. Applicant cancels claims 11, 12 and 18 without prejudice. Applicant amends claims 10, 17, and 19-21 of the present application; marked up versions of the amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). Claims 10, 17 and 19-21 are pending in the application. Reexamination and reconsideration of the application are respectfully requested.

The Examiner objects to the title of the invention as non-descriptive. Applicant amends the title to address this objection. The Examiner objects to FIG. 1-19 as informal. Applicant submits proposed new FIG. 1-19 with amendments indicated in red on the attached sheets, as proposed figures to address this objection. Moreover, the Examiner objects to the specification as informal.